

WHAT IS CLAIMED IS:

- 1 1. In an integrated circuit multichannel packet transfer device, an apparatus
2 for transferring a plurality of data packets, comprising:
3 a first interface circuit for receiving packet data on a first channel;
4 a memory;
5 a packet manager circuit coupled between the first interface circuit and the
6 memory to receive data on the first channel from the first interface circuit, wherein the
7 packet manager circuit is configured to write at least a first data packet fragment to the
8 memory under control of a first descriptor, and is configured to write at least a second
9 data packet fragment to the memory under control of a second descriptor;
10 a timer for generating a first time-out signal at a predetermined time after the first
11 descriptor is ready for transfer; and
12 a controller for controlling descriptor write back operations to memory in either
13 read-modify-write mode or write-invalidate mode, wherein the controller writes a
14 plurality of descriptors together to memory in a single write-invalidate operation if the
15 plurality of descriptors is ready for transfer before the first time-out signal is generated.
- 1 2. The apparatus recited in claim 1, wherein the controller writes the plurality
2 of descriptors separately to memory as a sequence of read-modify-write operations if the
3 plurality of descriptors is not ready for transfer before the first time-out signal is
4 generated.
- 1 3. The apparatus recited in claim 1, wherein the timer comprises
2 a multi-bit counter,
3 a multiplexer having one select line, one output and multiple inputs, with
4 each input coupled to a corresponding bit of the multi-bit counter,
5 a timer control register coupled to the select line of the multiplexer, and
6 a first pulse generator coupled to the multiplexer output for generating the
7 first time-out signals,

8 wherein the multiplexer selects one of the bits in the multi-bit counter for output
9 to the pulse generator in response to the timer control register to generate the first time-
10 out signal.

1 4. The apparatus recited in claim 1, where the memory comprises a cache
2 memory having a line width of $2N$, and the first and second descriptors each have a width
3 of N .

1 5. The apparatus recited in claim 1, where the memory comprises a system
2 memory and a cache memory, such that the packet manager writes data packets or
3 descriptors to the system memory or cache memory.

1 6. The apparatus recited in claim 1, further comprising a register for storing a
2 minimum descriptor count, whereby the controller writes a plurality of descriptors
3 together to memory in a single write-invalidate operation only if the plurality of
4 descriptors that are ready for transfer meets or exceeds the minimum descriptor count.

1 7. The apparatus recited in claim 1, where the timer comprises a memory
2 device for programmably storing a timer setting to selectively determine the
3 predetermined time at which the first time-out signal is generated.

1 8. The apparatus recited in claim 1, comprising:
2 a second interface circuit for transmitting packet data on a second channel;
3 an packet manager output circuit coupled between the memory and the second
4 interface circuit to transmit data from the memory on the second channel, wherein the
5 packet manager output circuit is configured to write output data packets to the second
6 interface circuit under control of a plurality of output descriptors;
7 a timer for generating a second time-out signal a predetermined time after a first
8 output descriptor is ready for transfer; and
9 a output controller for controlling output descriptor write back operations to
10 memory in either read-modify-write mode or write-invalidate mode, wherein the output
11 controller writes a plurality of output descriptors together to memory in a single write-

12 invalidate operation if the plurality of output descriptors is ready for transfer before the
13 second time-out signal is generated.

1 9. The apparatus recited in claim 8, wherein the output controller writes the
2 plurality of output descriptors separately to memory as a sequence of read-modify-write
3 operations if the plurality of output descriptors is not ready for transfer before the second
4 time-out signal is generated.

1 10. A data transfer controller for managing the direct memory transfer of data
2 on a first channel by releasing one or more descriptors associated with said first channel,
3 where said data transfer controller is coupled to receive a time-out pulse for the first
4 channel and is configured to delay release of said one or more descriptors until after
5 receiving the time-out pulse for the first channel.

1 11. The data transfer controller recited in claim 10, wherein a plurality of
2 descriptors received before the time-output pulse is generated are released together with a
3 write-invalidate command.

1 12. The data transfer controller recited in claim 10, wherein a plurality of
2 descriptors are released sequentially with read-modify-write commands when only one of
3 the plurality of descriptors is received before the time-output pulse is generated.

1 13. The data transfer controller recited in claim 10, comprising a timer for
2 generating a time-out pulse at a predetermined time interval after a first of the plurality of
3 descriptors is received.

1 14. The data transfer controller recited in claim 13, wherein the predetermined
2 time interval may be programmably selected from a plurality of timer interval values.

1 15. The data transfer controller recited in claim 10, comprising a packet
2 manager input circuit for transferring a plurality of packets to memory under control of
3 said one or more descriptors.

1 16. The data transfer controller recited in claim 10, comprising a packet
2 manager output circuit for transferring a plurality of packets from memory under control
3 of said one or more descriptors.

1 17. A method comprising:
2 receiving a first packet fragment in an interface circuit;
3 receiving a second packet fragment in the interface circuit;
4 transmitting the first and second packet fragments from the interface circuit to a
5 memory under control of the first and second descriptors, respectively;
6 setting a timer to expire a predetermined time interval after the first descriptor for
7 the first packet fragment is released; and
8 writing the first and second descriptors back to memory together as a write-
9 invalidate command if the second descriptor is released before expiration of the timer.

1 18. The method recited in claim 17, further comprising writing the first and
2 second descriptors back to memory separately as a sequence of read-modify-write
3 commands if the second descriptor is not released before expiration of the timer.

1 19. The method recited in claim 17, wherein the first and second descriptors
2 are written back to a cache memory having a line width of $2N$, and the first and second
3 descriptors each have a width of N .

1 20. The method of claim 19, wherein the first and second descriptors are
2 written back to a cache memory having a line width of $32B$, and the first and second
3 descriptors each have a width of $16B$.